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IEE CNF IEEE STD	IEE Conference Proceeding		Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 8, Issue 1, Feb. 2000 Page(s):18 - 29
	IEEE Standard		Digital Object Identifier 10.1109/92.820758 <u>AbstractPlus References </u> Full Text: <u>PDF(</u> 300 KB) IEEE JNL
			 Analytical models for RTL power estimation of combinational and sequer Gupta, S.; Najm, F.N.; Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions Volume 19, Issue 7, July 2000 Page(s):808 - 814 Digital Object Identifier 10.1109/43.851996
			AbstractPlus References Full Text: PDF(212 KB) IEEE JNL
			3. Energy and peak-current per-cycle estimation at RTL Gupta, S.; Najm, F.N.; Very Large Scale Integration (VLSI) Systems, IEEE Transactions on
			Volume 11, Issue 4, Aug. 2003 Page(s):525 - 537 Digital Object Identifier 10.1109/TVLSI.2002.800534
			AbstractPlus References Full Text: PDF(721 KB) IEEE JNL
			4. Power macro-models for DSP blocks with application to high-level synthe Gupta, S.; Najm, F.N.; Low Power Electronics and Design, 1999. Proceedings. 1999 International Syn 1999 Page(s):103 - 105
			AbstractPlus Full Text: PDF(228 KB) IEEE CNF
			5. Energy-per-cycle estimation at RTL Gupta, S.; Najm, F.N.; Low Power Electronics and Design, 1999. Proceedings. 1999 International Syr 1999 Page(s):121 - 126
			AbstractPlus Full Text: PDF(448 KB) IEEE CNF
			6. Analytical model for high level never modeling of combinational and com-

Gupta, S.; Najm, F.N.;

4-5 March 1999 Page(s):164 - 172

Analytical model for high level power modeling of combinational and seq

Low-Power Design, 1999. Proceedings. IEEE Alessandro Volta Memorial Worl

Digital Object Identifier 10.1109/LPD.1999.750417

<u>AbstractPlus</u> | Full Text: <u>PDF</u>(6012 KB) **IEEE CNF**

7. Power Macromodeling For High Level Power Estimation

Gupta, S.; Najm, F.N.;

Design Automation Conference, 1997. Proceedings of the 34th

June 9-13, 1997 Page(s):365 - 370

AbstractPlus | Full Text: PDF(572 KB) IEEE CNF

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